EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(emulat$3 adj (memory or cache)) same ((seperat$3 or independent) near2 (interface or bus))	US-PGPUB; USPAT	OR	ON	2006/10/10 15:14
L2	23	(emulat$3 adj (memory or cache))and ((seperat$3 or independent) near2 (interface or bus))	US-PGPUB; USPAT	OR	ON	2006/10/10 15:14
S1	302	711/?.ccls. and emulat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:25
S2	38821	S1 and instruct$3 or operand or op$code	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:11
S3	184	S1 and (instruct$3 or operand or op$code)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:12
S4	138	S3 and compar$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:12
S5	55	S1 and (instruct$3 and (operand or op$code))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:13
S6	41	S5 and compar$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:13
S7	7934	(emulat$ same ((memory or cache) and (process$3 or controller)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:27
S8	606	S7 and (operand and op$code)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:28
S9	15	S7 and (independent same (operand and op$code))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:37

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S10	241	emulat$3 adj2 (memory and process$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:38
S11	0	(emulat$3 adj2 (memory and process$3)) and ((op$code and operand)near (interface or data))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 11:39
S12	28	(emulat$3 adj2 (memory and process$3)) and ((op$code and operand))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:04
S13	23791	(emulat$4 same (process$3 or microprocess$3 or controller))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:06
S14	8385	(emulat$4 same ((process$3 or microprocess$3 or controller) and (memory or cache)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:06
S15	3672	(emulat$4 same ((process$3 or microprocess$3 or controller) and (memory or cache))) and (instruction and logic)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:08
S16	2661	(emulat$4 same ((process$3 or microprocess$3 or controller) and (memory or cache))) and (instruction and logic) and compar$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:07
S17	2424	(emulat$4 same ((process$3 or microprocess$3 or controller) same (memory or cache))) and (instruction and logic) and compar$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:07
S18	303	(emulat$4 same ((process$3 or microprocess$3 or controller) same (memory or cache))) same (instruction and logic) and compar$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:08
S19	560	(emulat$4 same ((process$3 or microprocess$3 or controller) and (memory or cache))) and (instruction and logic) and (operand and op$code)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:08

EAST Search History

S20	108	(emulat$4 same ((process$3 or microprocess$3 or controller) same (memory or cache))) same (instruction and logic) and compar$4 and (op$code and operand)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:09
S21	15	(emulat$4 same ((process$3 or microprocess$3 or controller) same (memory or cache))) same (instruction and logic) and compar$4 and ((op$code and operand) same (data and pointer))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:15
S22	312	(711/2).CCLS.	USPAT; USOCR	OR	OFF	2006/10/10 12:15
S23	188	(711/123).CCLS.	USPAT; USOCR	OR	OFF	2006/10/10 12:16
S24	358	(711/129).CCLS.	USPAT; USOCR	OR	OFF	2006/10/10 12:16
S25	159	(711/214).CCLS.	USPAT; USOCR	OR	OFF	2006/10/10 12:16
S26	16	S22 and (emulat$4 same ((process$3 or microprocess$3 or controller) and (memory or cache)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:26
S27	1	S22 and (emulat$4 adj (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:26
S28	0	S23 and (emulat$4 adj (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:26
S29	1	S23 and (emulat$4 adj2 (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:27
S30	3	S22 and (emulat$4 adj2 (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:28
S31	1	S24 and (emulat$4 adj2 (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:29
S32	1	S25 and (emulat$4 adj2 (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:29

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S33	1323	(emulat$4 adj2 (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 12:29
S34	969	(emulat$4 adj2 (memory or cache))	US-PGPUB; USPAT	OR	ON	2006/10/10 12:30
S35	108	(emulat$4 adj2 (memory or cache)) and (op$code and operand)	US-PGPUB; USPAT	OR	ON	2006/10/10 12:30
S36	4	(emulat$4 adj2 (memory or cache)) same(op$code and operand)	US-PGPUB; USPAT	OR	ON	2006/10/10 12:31
S37	99	(emulat$4 adj2 (memory or cache)) and (op$code and operand) and compar$5	US-PGPUB; USPAT	OR	ON	2006/10/10 12:33
S38	87	(emulat$4 adj2 (memory or cache)) and (op$code and operand) and compar$5 and pointer	US-PGPUB; USPAT	OR	ON	2006/10/10 12:36
S39	3	(emulat$4 adj2 (memory or cache)) and ((op$code and operand) same (pointer and interface))and compar$5	US-PGPUB; USPAT	OR	ON	2006/10/10 12:33
S40	85	(emulat$4 adj2 (memory or cache)) and (op$code and operand) and compar$5 and pointer and (write and read)	US-PGPUB; USPAT	OR	ON	2006/10/10 12:36
S41	42	(emulat$4 adj2 (memory or cache)) and (op$code and operand) and compar$5 and pointer same (write and read)	US-PGPUB; USPAT	OR	ON	2006/10/10 12:37
S42	165	(emulat$4 adj2 (memory or cache)) same (read and write)	US-PGPUB; USPAT	OR	ON	2006/10/10 12:38
S43	57	(emulat$4 adj2 (memory or cache)) same (read and write) same interface	US-PGPUB; USPAT	OR	ON	2006/10/10 12:38
S44	20	(emulat$4 adj2 (memory or cache)) same (read and write) same interface and (op$code and operand)	US-PGPUB; USPAT	OR	ON	2006/10/10 12:38
S45	11649	(emulat$4 same (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 13:36
S46	1138	(emulat$4 near (memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 13:36
S47	659	(emulat$4 adj(memory or cache))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 13:36
S48	0	(emulat$4 adj(memory or cache)) same ((independent or separat$3) near interface)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 13:37
S49	23	(emulat$4 adj(memory or cache)) same ((independent or separat$3) same (interface and data))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/10 14:16
S50	0	indpendent near (op$code and operand)	US-PGPUB; USPAT	OR	ON	2006/10/10 14:17

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S51	0	independent near (op$code and operand)	US-PGPUB; USPAT	OR	ON	2006/10/10 14:17
S52	3	((independent or separat$3) near (op$code and operand))	US-PGPUB; USPAT	OR	ON	2006/10/10 14:23
S53	2025	((emulat$4 or simulat$4) near (memory or cache))	US-PGPUB; USPAT	OR	ON	2006/10/10 14:23
S54	3	((emulat$4 or simulat$4) near (memory or cache)) same (op$code and operand)	US-PGPUB; USPAT	OR	ON	2006/10/10 14:49
S55	135	(emulat$4 with (memory or cache)) and (fetch$3 same (op$code and operand))	US-PGPUB; USPAT	OR	ON	2006/10/10 15:01
S56	20	(emulat$4 adj (memory or cache)) and (fetch$3 same (op$code and operand))	US-PGPUB; USPAT	OR	ON	2006/10/10 15:03
S57	3	(emulat$4 adj (memory or cache)) and (fetch$3 near2 (op$code and operand))	US-PGPUB; USPAT	OR	ON	2006/10/10 15:03
S58	3	(emulat$4 adj (memory or cache)) and ((fetch$3 or access$3) near2 (op$code and operand))	US-PGPUB; USPAT	OR	ON	2006/10/10 15:03

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☐	L1	(emulat$ adj (memory or cache))	308

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#4	((emulated and (memory or cache) and data and instruction) <in>metadata)	2
#5	((emulated and (memory or cache) and data and instruction) <in>metadata)	2
#6	((emulated and (memory or cache) and data and instruction) <in>metadata)	2
#7	((((emulated or emulator or emulating or emulation or simulating or simulation or simulator or simulated) and (processing or processor or microprocessor or microprocessing) and (memory or cache)) and data and instruction)<in>metadata)	218
#8	((((emulated or emulator or emulating or emulation or simulating or simulation or simulator or simulated) and (processing or processor or microprocessor or microprocessing) and (memory or cache)) and data and instruction)<in>metadata)	218
#9	((((emulated or emulator or emulating or emulation or simulating or simulation or simulator or simulated) and (processing or processor or microprocessor or microprocessing) and (memory or cache)) and data and instruction)<in>metadata)	218
#10	((independent read request)<in>metadata)	0
#11	((independent and (fetch or access) and (opcode and operand)) <in>metadata)	0

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Skeppstedt, J.; Dubois, M.;
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2. **A decentralized virtual memory scheme implemented on an emulated multiprocessor**
Brorsson, M.;
System Sciences, 1989. Vol.I: Architecture Track, Proceedings of the Twenty-Second Annual Hawaii International Conference on
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emulated AND memory AND (opcode and operand) Search

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...instruction, the right **operand** is the source and the left **operand** is the destination. For...mnemonic identifier of an **opcode**, EAX is the destination **operand**, and SUBTOTAL is the...addressing. This means **memory** is organized and accessed...
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This directive can redefine an existing **opcode** name or create a new one. ... The first character specifies the **operand access** type, and the second character ...
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For each **opcode**, this class provides a method whose arguments are the valid ... on a **separate** and **independent** form and provides a class to **access** just the ...
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